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COMPUTER SIMULATION OF PHOTOCURRENTS IN P-N JUNCTIONS USING RADSPICE

by

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ABSTRACT

Computer simulation of radiation effects in electronics is an important research and engineering tool for understanding the interaction of nuclear and space radiation in semiconductor devices and for developing rad-hard electronics at the device, circuit and system level. This report investigates the photocurrent modelling capability of a commercially available SPICE circuit simulation code (RADSPICE) that has integrated radiation effects modelling capability. Specifically, the various models for photocurrent generation in p-n junctions from pulses of ionizing radiation are discussed and sample simulations are provided for each of the photocurrent models. The simulation results are compared with theoretical values and the limitations of the models and range of applicability are discussed.

Single-event upset (SEU) modelling in a CMOS static random access memory (SRAM) is illustrated using photocurrent simulation techniques. A corresponding rad-hard version of the SRAM is demonstrated. RADSPICE simulation results for both non-rad-hard and rad-hard SRAM designs are evaluated, thereby providing a means of estimating SEU vulnerability.

RÉSUMÉ

Les codes machines qui peuvent être utilisé pour simuler les effets des radiations nuclaires et interstellaires dans les appariels et les circuits électroniques sont très importants pour comprendre les actions réciproques de ces radiations dans ces choses électroniques. Aussi, avec les codes machines, nous pouvons créer une mode pour la défense des apppariels et des circuits électroniques contre les effets des radiations nuclaires et interstellaires. Ce rapport considére la capacité des codes machines SPICE et RADSPICE pour simuler les effets de ces radiations dans ces choses électroniques. Precisément, nous discoutons les modèles être utilisé pour simuler la génération des photocourants électroniques dans les junctions p-n comme suite aux impulsions des radiations ionisant. Les résultats des simulations sont mettre en contraste avec les valeurs théoretiques. Ensuite, nous presentons les limitations et les champs d'applications approprié a SPICE et RADSPICE.

Création des modèles "SEU" (un appareil électronique qui vient d'avoir un coup électronique, émanent d'un stimulus du dehors) dans les elements CMOS SRAM (mémoire statique d'accès au hasard) a été fait, un comme l'autre, pour les appareils sensibles et les appareils insensibles à SEU. Les resultats de ces simulations sont evalueés, en fournir l'utilisateur avec une modalité de faire une idéé exacte de la vulnerabilité aux SEU.

EXECUTIVE SUMMARY

Computer-aided engineering (CAE) tools such as SPICE (Simulation Program with Integrated Circuit Emphasis) have been successfully used for almost three decades to simulate the electrical performance of electronic devices and circuits. One such simulation program, RADSPICE, has the added feature of being able to simulate a useful range of radiation effects in electronics. This report investigates the simulation techniques used in RADSPICE for modelling photocurrents produced by the interaction of ionizing radiation in p-n junctions. Using photocurrent modelling techniques, a method for creating and simulating a radiation hardened (for space radiation effects) complementary metal oxide semiconductor (CMOS) static random access memory (SRAM) is illustrated.

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1.0 INTRODUCTION

Computer-aided engineering (CAE) software tools such as SPICE (Simulation Program with Integrated Circuit Emphasis) have found wide acceptance and use by the engineering and scientific community for reliable simulation of electrical circuit response to various stimuli. Since SPICE was first released in 1975 by the Electronics Research Laboratory of the University of California, various institutions and commercial software houses have continually expanded the range of modelling capabilities and have improved the user interface. More recently, the ability to simulate the effects of ionizing radiation on circuit and individual component behaviour has been implemented, with the computer code being renamed to reflect the new feature (e.g. RADSPICE). This report discusses the ability of these SPICE-like computer codes (hereafter referred to generically as SPICE codes) to model radiation effects in semiconductors.

The addition of radiation effects modelling to SPICE computer codes has created a time and cost-saving tool for engineers involved in the design of radiation hardened (rad-hard) semiconductor components and circuits. These codes have reduced the guesswork, reliance on "rules-of-thumb" and dependence on prohibitively expensive test protocols routinely used to predict the response of devices and circuits to radiation of man-made (e.g. from nuclear weapons) and natural (e.g. space radiation) origin. In addition, SPICE codes have been both developed and used by researchers in radiation effects on electronics to predict and quantify the results of the interaction of various forms of nuclear radiation with semiconductor devices. In order to successfully utilize these computer codes for both engineering and scientific applications, a basic understanding of both the modelling techniques used by the codes and the permissible range of application is required. In addition, an understanding of how the models have been implemented (i.e. in the software source code) is sometimes necessary to explain questionable simulation results, or, the apparent non-convergence of a solution for some aspect of a simulation.

Recently, Defence Research Establishment Ottawa (DREO) acquired a commercial circuit simulation software package "HSPICE" and an optional module "RADSPICE" (both HSPICE and RADSPICE are trademarks of Meta-Software, Inc., Campbell, Ca, U.S.A.), the latter of which is used to simulate the effect of radiation on electronics. The models used for simulating the

interaction of radiation with semiconductor devices and the resulting electrical response were partially developed and incorporated into RADSPICE by Science Applications International Corporation (SAIC). The intended application of RADSPICE at DREO includes support of experimental work in radiation effects on electronics and to assist in development of radiation hardening expertise at the component, circuit and system level.

This work discusses and illustrates by way of example a partial range of radiation effects simulation that HSPICE/RADSPICE provides and describes the pitfalls and limitations inherent in using the RADSPICE models. In particular, the photocurrent modelling capability of RADSPICE for p-n junctions is discussed. The intent of this report is not to illustrate how to use RADSPICE, rather, to illustrate the possible range of applications of the code, some of which are part of on-going work at DREO. Also demonstrated through simulation is a single-event upset (SEU) hardening technique for a CMOS static RAM at the integrated circuit level, which also requires photocurrent modelling. A simple simulation is presented for each of the radiation modelling techniques discussed. A future DREO report will discuss the remaining radiation effects modelling techniques available with RADSPICE (see section 3.0 for a brief description).

2.0 MODELLING RADIATION EFFECTS IN SEMICONDUCTORS USING SPICE

The most widely studied and well-understood radiation effect on electronics is the passage of ionizing radiation through semiconductor devices, in particular for p-n junctions. The subsequent generation of electron-hole pairs, diffusion and collection of charge within a device can result in an external photocurrent. Any SPICE program capable of simulating a time-dependent current source is capable of simulating this phenomena via an empirical approach.

As an example, consider a circuit composed of several active semiconductor devices. The transient photocurrent responses of the active semiconductor devices, under given bias conditions, can be individually or collectively measured for a real ionizing radiation pulse of interest (i.e. specifying the pulse-shape and dose rate). For the same set of bias conditions, SPICE can be

used to "simulate" circuit response for the same radiation pulse by assigning a time-dependent current source to each active component in the circuit. The inclusion of the current source simulates the photocurrent time-history before, during and after the ionizing radiation pulse. If a database of semiconductor component response data is available (containing their individual transient radiation response data for a variety of irradiation and bias conditions), then in principle, any circuit utilizing any combination of these components can be simulated.

If the particular implementation of the SPICE code permits the compilation and linking of user subroutines (usually written in FORTRAN or C) with the main code, then photocurrents and/or other radiation effects (e.g. total dose effects) can be simulated. However, this is usually not a trivial task. By selecting a particular radiation response model rather than relying on empirically determined or measured radiation response data, the SPICE code will have general application for a variety of devices and will not be device specific. For example, the Wirth-Rogers [1] model of photocurrent generation in a p-n junction for a square pulse of ionizing radiation could be implemented. This would apply only for devices containing a p-n junction, such as diodes and bipolar junction transistors (BJTs).

The most accurate radiation response simulations are performed using the empirical (i.e. experimental) approach. However, all encompassing device databases are not available and the process of making experimental measurement of device response for every new simulation is self-defeating. It is also a difficult and time-consuming task if the analyst attempts to incorporate the semiconductor device radiation response models developed by others into SPICE. In practice, a combination of both techniques is routinely used for simulation of radiation effects on electronics.

In order to reduce development time, commercial SPICE software packages were evaluated that claimed to have semiconductor device radiation response modelling capability. HSPICE/RADSPICE was acquired by DREO because it afforded the widest range of "built-in" radiation effects simulation capability (including theoretically derived models) and also allowed empirically derived response data to be used.

3.0 SEMICONDUCTOR DEVICE RESPONSE MODELLING USING RADSPICE

Active semiconductor components are normally the circuit elements which are the most sensitive to the effects of ionizing radiation, with passive elements being the least sensitive. The primary method for incorporation of radiation effects into RADSPICE was to augment the electrical models for active circuit elements with electrical parameters that are affected by various levels and types (e.g. ionizing and non-ionizing) of nuclear radiation. The two types of radiation effects modelled in RADSPICE, which are also of the most concern to the military, are total dose effects and transient photocurrents (dose rate effects) in p-n junctions.

Total dose effects in semiconductor devices generally result in permanent degradation and/or device failure. Total dose effects are modelled in RADSPICE for MOSFETs only. Only one device modelling option is available in RADSPICE which allows for linear degradation of three important MOSFET parameters; the threshold voltage, the low-field mobility and the fast surface state density.

Photocurrent effects are modelled in diodes, bipolar junctions transistors (BJTs), junction field effect transistors (JFETs), metal-semiconductor field effect transistors (MESFETs) and metal oxide field effect transistors (MOSFETs), with a variety of modelling options available for photocurrent generation in these devices. This report includes photocurrent modelling in p-n junctions and simplified photocurrent modelling in MOSFETs for SEU simulation.

3.1 PHOTOCURRENT MODELLING IN P-N JUNCTIONS

RADSPICE provides the analyst with both theoretical and empirical approaches to photocurrent modelling in semiconductor devices. With any of the modelling approaches there are two global options that can be selected. The first option allows photocurrent generation in all p-n junctions, with the exception of BJTs; i.e. only the collector-base junction generates photocurrent. The second option expands upon the first to include photocurrents generated in the emitter-base junction of the BJT. The two options are useful in the case where bipolar

circuitry is analyzed. The collector-base photocurrent can sometimes bias a transistor ON under certain conditions, whereas the emitter-base photocurrent can either enhance or suppress this phenomena. With RADSPICE, the emitter-base photocurrent can be turned OFF/ON to assess the above effect.

In RADSPICE the ionizing radiation source generating the photocurrent in the p-n junction must be specified in terms of dose rate as a function of time. Any of the RADSPICE independent source functions may be used to specify the time history of the radiation pulse. These functions include PULSE, EXP (exponential), SIN (sinusoidal), PWL (piece-wise linear) and SFFM (single-frequency modulation function). In practice, the SIN and SFFM functions are of little practical use for describing time histories of ionizing radiation "pulses", since they describe unrealistic pulse shapes. A maximum of nine different independent ionizing radiation sources may be specified per simulation.

Figure 1 indicates the modelling approach used by RADSPICE for generating photocurrents in p-n junctions. An independent photocurrent source (I_{pp}) is placed in parallel with each p-n junction in the circuit. The time history of the photocurrent source(s) will depend on the physical and electrical parameters input into RADSPICE. These parameters describe 1) the time history of the ionizing radiation source, 2) the photocurrent generation model and 3) the electrical and physical data representing the p-n junction(s), with the latter two sets of parameters affected by circuit bias conditions. Each device model describing active components in the circuit (e.g. diode, BJT, etc.) requires a set of model parameters to enable RADSPICE to simulate the radiation response. The photocurrent model is selected by the parameter RLEV in the simulation input file. For a given semiconductor device, the number of model parameters required can differ for each of the photocurrent models.

In sections 3.1.1 through 3.1.3 we will briefly discuss each of the five photocurrent models employed in RADSPICE, and illustrate them with a brief example.

3.1.1 WIRTH-ROGERS PHOTOCURRENT MODEL

The Wirth-Rogers analytical model (RLEV=1) has been used extensively in simulation work and is described in detail elsewhere [1]. The restrictions for applying this model are;

1. The ionizing radiation pulse must be square (i.e. negligible pulse rise and fall times relative to the pulse width).
2. The ionizing radiation is sufficiently penetrating to produce uniform ionization throughout the junction.
3. The voltage across the p-n junction remains fixed throughout the simulation.
4. The junction is abrupt, one-sided and the doping level is constant.

In many simulations these are valid assumptions and are useful in cases where they are accurate only as first-order approximations. The Wirth-Rogers closed-form solution contains two terms; the first is responsible for the turn-on and build-up of the photocurrent during the radiation pulse and the second term provides for the turn-off and decay of the photocurrent after the pulse ends. Each of the terms is composed of a prompt and a delayed component. The prompt component arises from electron-hole pairs generated in the depletion layer and collected under the influence of the applied electric field. The delayed or drift photocurrent component arises from carriers generated outside of the depletion layer which then diffuse into the depletion layer and add to the prompt component of the photocurrent.

A RADSPICE simulation was conducted using the Wirth-Rogers model for a reverse biassed diode subjected to a 200 ns wide square pulse of ionizing radiation (dose rate=1×10^{9} rads(Si)/s), using the following parameters required for a LEVEL 1 diode model;

diode junction area	AREA=1×10^{-8} m^2
diffusion length	DIFL=50 nm
zero bias junction capacitance per unit junction bottom-wall area	CJO=7.35×10^{-3} F
diffusion current time constant	TD=50 ns
area junction grading coefficient (default value)	M=0.5

area junction contact potential
(default value) PB=0.8 V

The results of the simulation are shown in Figure 2, for reverse bias voltages of 20, 10 and 2 volts. Also shown is the result for 10 volts reverse bias and zero diffusion length (DIFL=0). This case was included to assist in verification of the simulation results through comparison with theoretical values. The ionizing radiation pulse began at t=5 ns and has negligible fall and rise times (both 0.1 ns). The three curves for DIFL=50 nm illustrate the expected behaviour; for increasing reverse bias voltage the photocurrent increases. As the reverse bias voltage increases, the depletion width increases and thus the charge-collection volume for the prompt photocurrent increases. The delayed photocurrent arises (in the Wirth-Rogers model) from the volume that extends one diffusion length from the boundary of the depletion region and is, therefore, independent of changes in the depletion width (and hence, bias conditions). The contribution of the delayed photocurrent can be observed from the difference in the two photocurrent response curves for the 10 volt reverse bias condition. There is zero delayed component of the photocurrent for DIFL=0, but for DIFL=50 nm, the peak diffusion current is approximately equal in magnitude to the prompt photocurrent. As will be shown, the diffusion length and associated time constant were selected to yield a peak diffusion (delayed) photocurrent current approximately equal to the prompt photocurrent.

To determine the depletion width, the junction capacitance and the junction area must be known. The simple parallel plate capacitor model is used to determine the depletion width W, i.e.

$$W = \epsilon_r \, \epsilon_0 \, A_{eff} / C \qquad (1)$$

where ϵ_r is the permittivity of free space (8.85×10^{-12} F/m), ϵ_0 is the relative permittivity of the semiconductor material (11.4 for Si), A is the effective junction area (m^2) and C is the capacitance (F). In HSPICE/RADSPICE, the "real" junction area A is scaled by the parameter M (as are many other diode parameters), described above, thus $A_{eff}=A \cdot M$. Using reasonable values of C=20 pF and A=AREA=1×10^{-8} m^2 (100 μm x 100 μm), the depletion width W=50 nm.

To determine the input parameter CJO, the following formula is used [2] for a reverse biassed ($V_{bias}<0$) diode

$$C = CJO_{eff}\ (1-V_{bias}/PB)^{-M} + CJP_{eff}(1 - V_{bias}/PHP)^{-MJSW}\ , \qquad (2)$$

where

CJP_{eff} = effective zero-bias junction capacitance per unit junction periphery (for level 1 diode $CJP_{eff} = CJP \cdot M$),
PHP = periphery junction contact potential and
MJSW = periphery junction grading coefficient.

Since $CJP_{eff}=0$ (default value for a LEVEL 1 diode model), the right-hand term of equation 2 is zero and the values of PHP and MSJW are not required for the simulation or the subsequent analysis. Simplifying equation 2 yields

$$C = CJO_{eff}\ (1-V_{bias}/PB)^{-M} = CJO\ M\ (1-V_{bias}/PB)^{-M}\ . \qquad (3)$$

and solving for CJO yields

$$CJO = C\ (1-V_{bias}/PB)^{M}/M\ . \qquad (4)$$

For $V_{bias}=-10$ volts, C=20 pF and PB=0.8 volts, $CJO=7.35\times10^{-3}$ F. From the Wirth-Rogers model, the prompt photocurrent (in Amperes) is given by

$$I_{pp\text{-}prompt} = q\dot{\gamma}gAW\ u(t-t_s),\ \text{for } t<\text{duration of pulse} \qquad (5)$$

where
q = electronic charge = 1.6×10^{-19} C,
$\dot{\gamma}$ = dose rate (rads(Si)/s),
g = carrier generation constant
= 4.2×10^{19} carriers/rad m^3 (for silicon),
A = junction area (m^2),
W = depletion width (m^2),
u = unit step function and
t_s = the start of the ionizing radiation pulse (s).

The delayed photocurrent (in Amperes) for the Wirth-Rogers model is given by

$$I_{pp\text{-}delayed} = q\dot{\gamma}gAL\ \mathrm{erf}[(t-t_s)/\tau]^{1/2}u(t-t_s), \qquad (6)$$
for t<duration of pulse,

where, additionally,

L = diffusion length (m) ≡ DIFL,
τ = diffusion time constant (s) ≡ TD and
erf = error function.

Substituting the simulation values into the above equations, theoretical application of the Wirth-Rogers model predicts $I_{pp\text{-}prompt}$=3.39 μA and for t→205 ns (the end of the 200 ns wide ionizing radiation pulse) $I_{pp\text{-}delayed}$=3.36 μA. The RADSPICE simulation results were 3.49 μA and 3.34 μA, respectively, in good agreement with calculated values.

It should be noted that several radiation effects parameters seem to be implemented incorrectly or are documented incorrectly in RADSPICE. The parameter AJ represents the junction area for radiation effects modelling only and is documented to be independent of the parameter AREA, the junction area for electrical modelling. It was found that the photocurrent determined through RADSPICE simulation is independent of the value of AJ and depends on AREA only. In the previous analysis for determining the magnitude of the photocurrent, it was found that there was inconsistent use of the junction area (A) and the effective junction area (i.e. A_{eff}) for electrical and photocurrent modelling. Although the previous analysis is relatively simplistic, considerable effort was expended determining the relationship between the input parameters and the simulation results, as access to the RADSPICE source code is not possible due to the current software licensing agreement. Next, in the example diode photocurrent test cases supplied by Meta-Software for the Wirth-Rogers photocurrent model, it is implied that the parameters GENS (radiation current generation rate, C/rad), TDS (radiation deep storage time, s) and FDEP (prompt photocurrent fraction of the total photocurrent) must be specified for the simulation. These parameters are not required for the Wirth-Rogers model, but are required for other photocurrent models (RLEV=4, 5 and 6, which will be discussed subsequently). Finally, for large dose rates (>1x10^{11} rads(Si)/s), simulation execution times became unmanageably long because the RADSPICE internal time-step was changed from the preselected value (0.5 ns) to a prohibitively small value (<10^{-15} s). The source of this error has not been determined.

To illustrate a case where the Wirth-Rogers photocurrent solution is invalid, a simulation similar to the previous case was performed, but the diode was reverse biassed at 1.5 volts and a 200 ohm resistor was placed in series with the diode. The square radiation pulse starts at t=20 ns and lasts 25 ns. The diode voltage as a function of time (shown in Figure 3) drops from 1.5 volts to approximately -0.2 volts during the pulse. For V<0 volts, the diode is forward biassed. Since the potential across the diode does not stay relatively constant during the ionizing radiation pulse, the Wirth-Rogers model cannot be applied, because the depletion width (W) varies with voltage.

3.1.2 USER-DEFINED (EMPIRICAL) PHOTOCURRENT MODEL

The user-defined empirical photocurrent model (RLEV=3) "simulates" a user-defined current source placed in parallel with the junction. This model requires specification of only the desired ionizing radiation pulse time history and the dose-rate-to-current multiplicative conversion factor RFAC (units of C/rad). Any of the intrinsic HSPICE/RADSPICE independent source functions can be used to describe the time history of the radiation pulse. This model is useful when an experimentally measured device response is to be used, or when the user wants to independently control the photocurrent. In principle, this is the same technique used to model SEU effects in section 3.2.

A simulation was performed using the same diode electrical parameters as in section 3.1.1, with a reverse bias voltage of 10 volts. The ionizing radiation pulse consisted of two consecutive square pulses as follows;

pulse 1 10 ns$\leq$t$\leq$110 ns, dose rate=1×10^{9} rads(Si)/s and
pulse 2 110 ns$\leq$t$\leq$220 ns, dose rate=2×10^{9} rads(Si)/s.

The pulse rise and fall times were both 0.1 ns. Using the value of RFAC=1×10^{11} C/rad(Si) specified in the simulation, the product $\dot{\gamma}\cdot$RFAC indicates peak photocurrents of 10 mA and 20 mA are expected for pulse 1 and pulse 2, respectively. The results of the simulation, shown in Figure 4, are in agreement.

3.1.3 SEMI-EMPIRICAL PHOTOCURRENT MODELS

The final three photocurrent models are semi-empirical models that differ only in the degree of approximation, therefore, they are treated together in this section. These photocurrent models have application in modelling experimental data for devices that have been exposed to pulsed ionizing radiation from a LINAC or flash x-ray machine. Similar to the previous photocurrent model, any of the intrinsic HSPICE/RADSPICE independent source description functions can be used to describe the time history of the radiation pulse.

The parameter RLEV=4 selects a photocurrent model with a delayed component only (no prompt component) and assumes a constant reverse bias junction voltage. The photocurrent is given by

$$I_{pp} = G\dot{\gamma}[1 - \exp(-t/\tau_{DS})] \qquad (7)$$

where G = current generation "rate" (C/rad) ≡ GENS,
$\dot{\gamma}$ = dose rate (rads/s) and
τ_{DS} = radiation "deep storage" time constant (s) ≡ TDS.

In equation 7 and the following equations for the remaining two photocurrent models, the time t=0 is assumed to be the start of the ionizing radiation pulse. Also, these equations are valid only for the duration of the radiation pulse. After the radiation pulse ceases, the prompt portion of the photocurrent immediately becomes zero and the delayed photocurrent decreases proportional to $\exp(-(t-t')/\tau_{DS})$, where t' signifies the end of the ionizing radiation pulse.

The photocurrent model invoked with RLEV=5 has a delayed component and a fixed prompt component, and also assumes a constant reverse bias junction voltage, given by

$$I_{pp} = G\dot{\gamma}[F_{DEP} + (1 - F_{DEP})(1 - \exp(-t/\tau_{DS}))], \qquad (8)$$

where F_{DEP} = relative magnitude of the prompt photocurrent component (dimensionless $0 \le F_{DEP} \le 1$) ≡ FDEP.

Note that the two photocurrent models represented by equations 7 and 8 are independent of bias voltage. The

electrical modelling of the circuit, however, remains bias sensitive.

The final photocurrent model (RLEV=6) has a delayed component and a prompt component, but allows an arbitrary (i.e. time-varying) reverse bias junction voltage, given by

$$I_{pp} = G\dot{\gamma}[\ \theta\ F_{DEP} + (1 - F_{DEP})(1 - \exp(-t/\tau_{DS}))], \qquad (9)$$

$$\theta = [(\varphi - V_j)/(\varphi + 10)]^M, \qquad (10)$$

where V_j = junction potential (volts), negative for reverse bias
φ = built in junction potential (volts) ≡ PB.

The dimensionless quantity θ represents the depletion layer width at an arbitrary voltage (V_j), normalized to its value at a reverse voltage of 10 volts, i.e.

$$\theta = W(V_j)/W(10V)\ . \qquad (11)$$

This quantity represents a scaling factor for the depletion width and, hence, the prompt photocurrent. The use of this technique provides for a more accurate simulation as the junction or bias voltage across the diode is likely to change during a radiation pulse, especially for high dose rates. Finally, the parameter CJO (zero bias junction capacitance per unit junction bottom-wall area) must be specified for this model (see section 3.1.1).

A RADSPICE simulation was conducted using the above photocurrent models (RLEV=4, 5 and 6) for the same diode configuration (i.e. 10 volts reverse bias and zero load resistance), with diode electrical parameters as in previous simulations, except for the RLEV=6 model, in which a reverse bias voltage of 2 volts was used. The additional parameter values required for this simulation were GENS=1×10^{-12} C/rad, TDS=20 ns and FDEP=0.5. The dose rate for the square ionizing radiation pulse was 1×10^{9} rads(Si)/s, with the pulse commencing at t=10 ns and continuing for 200 ns. The pulse rise and fall times were both 0.1 ns. The results of the simulation are shown in Figure 5.

The simulation results illustrating the (RLEV=4) photocurrent model for the delayed component only (shown in

Figure 5 as a solid curve) exhibit the expected behaviour indicated by equation 7, for the build-up of the photocurrent. There is an exponential rise in photocurrent controlled by the time constant τ_{DS}, which was 50 ns. The peak photocurrent is given by $G\dot{\gamma}=1x10^{-12}$ C/rad(Si)·$1x10^{9}$ rad(Si)/s=1.0 mA, which coincides with the simulation result. At the end of the photocurrent pulse, the current exponentially decays with τ_{DS}.

The simulation results for the photocurrent model with a fixed prompt component and a normal delayed component (RLEV=5) are shown in Figure 5, as a dotted curve. Since F_{DEP}=0.5 the peak magnitude of the fixed prompt component (from equation 8) is $I_{pp\text{-}prompt}=G\dot{\gamma}F_{DEP}$=0.5 mA. The delayed photocurrent fraction is scaled by $1-F_{DEP}$ and the peak value also equals 0.5 mA. These calculated values are in agreement with the simulation results. The rise and fall of the delayed photocurrent is exponential, governed by the time constant τ_{DS}. The prompt photocurrent follows the shape of the ionizing radiation pulse, therefore, it has a 0.1 ns rise and fall time.

The final photocurrent model (RLEV=6) simulation results are shown as the dashed curve in Figure 5. The prompt component is reduced substantially, due to its dependence on bias voltage. The delayed photocurrent component, however, is the same as in the other two simulations (0.5 mA), since the functional dependence is the same. Using the values of φ=2 volts, M=0.5 and PB=0.8 volts, with equation 10, θ=0.51. Thus, the peak magnitude of the prompt photocurrent is $G\dot{\gamma}\theta F_{DEP}$=0.255 mA, in agreement with the simulation results.

3.2 SINGLE-EVENT UPSETS IN CMOS STATIC RANDOM ACCESS MEMORY

Single-event upsets (SEUs) or "soft errors" can occur in a static random access memory (SRAM) following a strike by a sufficiently energetic ion. Such events are of particular consequence in space-borne electronics, due to the relative abundance of heavy ions present in the near-earth cosmic ray particle spectrum. Photocurrent generated by the passage of an ion through the semiconductor material near a sensitive node can change the node voltage and alter the logic state stored in the memory cell (bit). The magnitude and duration of the photocurrent and resulting voltage transient are critical for

determining the SEU threshold. The following example illustrates how a CMOS SRAM may be SEU hardened by the simple addition of decoupling or feedback resistors. RADSPICE is used to determine the sensitivity threshold of the original SRAM and the effectiveness of the hardened design against SEU.

The key components of a "typical" 1 bit SRAM cell are shown in Figure 6, without the support circuitry necessary for reading from, writing to, and addressing the cell (this portion of the circuitry is superfluous to the hardening discussion). The 1 bit cell consists of 2 cross-coupled CMOS inverters, forming a D-type flip-flop, with each inverter in turn composed of a p-channel and n-channel enhancement MOSFET. A 1 megabit SRAM would consist of 2^{20}=1,048,576 such cells of four MOSFETs each and the corresponding support circuitry. Although a 1 bit cell is modelled for this discussion, RADSPICE is capable of simulating more complex circuitry such as a 1 megabit SRAM.

The operation of the 1 bit SRAM cell is quite simple. Referring to Figure 6, a digital logic 1 or 0 (corresponding to a voltage level of 5 volts or 0 volts, respectively) is introduced to NODE 1 via external support circuitry. If a logic 1 is to be <u>written</u> to the cell then a 5 volt signal level must be applied to NODE 1, which turns M2 ON (n-channel MOSFET) and M4 (p-channel MOSFET) OFF. Note that NODE 2 is near ground because M2 is conducting, thereby biassing M3 on and M1 off and "reinforcing" the logic input of 1 (5V) at NODE 1. The data logic level during the <u>write</u> must be of sufficient duration for the circuit to settle in the above fashion. This is known as the "write hold time" or "data valid time". A similar sequence occurs for writing a logic 0 to the cell. In the above example, NODE 2 would contain the complement of the stored bit and would be inverted during a read operation by the support circuitry within the SRAM. For comparison, during a <u>read</u> operation the external circuitry would gate NODE 2 to circuitry external to the device.

In the previous example, the approach taken for SEU modelling with RADSPICE was to place a time-dependent current source ($I_{SEU}(t)$ in Figure 6) across the drain-source of the "target" MOSFET. The current source simulates the photocurrent produced within the MOSFET during ion traversal and subsequent charge collection. An SEU could occur for a hit at any of the four MOSFETs comprising the 1 bit SRAM cell, depending upon the

logic state stored in the cell, i.e. whether the target MOSFET was biassed ON or OFF. This example models an ion hit on the most sensitive element of the cell when a logic 1 is stored, i.e. a hit on M4 (p-channel MOSFET). Such a situation requires that M2 and M3 are biassed ON and M1 and M4 are OFF, hence, a logic 0 exists at NODE 2 (the complement of the bit written to the cell). If $I_{SEU}(t)$ is of sufficient magnitude and duration, M4 will conduct due to the ion strike and bias M1 ON, grounding NODE 1. This in turn biasses M2 OFF and M4 ON, setting NODE 2 to a logic 1, and indicating that a soft error has occurred.

The time-dependent ion induced photocurrent function $I_{SEU}(t)$ depends on many physical parameters related to the physics of the ion, the memory cell and their interaction. As the ion travels through the depletion layer and into the substrate, electron-hole pairs are created in the vicinity of the ion's track. The charge deposited in the sensitive volume surrounding transistor M4 depends on the path length of the ion trajectory, which varies as $\sec(\theta)$ (where θ is the angle-of-incidence with the die surface). The degree of ionization created in the sensitive volume is dependent on the ion's energy loss per unit path length (dE/dx), or linear energy transfer (LET). The LET is in turn dependent on the particle type (e.g. electron, proton, alpha particle, heavy ion, etc.) and energy. Charge collection and the resulting photocurrent production is a complicated process and is described elsewhere [3]. The photocurrent pulse shape, magnitude and duration are affected by such factors as the doping profile in the semiconductor and the distance from the sensitive node to the ion's trajectory in the sensitive volume.

An analytical approximation of the ion-induced time-dependent photocurrent ($I_{SEU}(t)$) is given by [3]

$$I_{SEU}(t) = I_0 \sec(\theta) \left[\exp(-t/\alpha) - \exp(-t/\beta)\right] , \qquad (12)$$

where I_0 is approximately the peak photocurrent for a given angle-of-incidence θ, α is the charge collection time constant of the junction and β is the time constant for initially establishing the ion track. I_0 is a scalable parameter which varies with cell size. For this simulation, typical values used for α and β were 150 ps and 40 ps, respectively [3]. Curves of $I_{SEU}(t)$ for a (fixed) arbitrary I_0 (normalized to the θ=0 curve) are shown in Figure 7, with θ=0, 15, 45, 60 and 75 degree angles-

of-incidence. To incorporate this function in the RADSPICE simulation, I_0 and sec(θ) were left as multiplicative parameters and the function [exp(-t/α) - exp(-t/β)] was modelled using a piece-wise linear function (PWL) with the above values for α and β. This technique was necessary since RADSPICE does not provide the user with a method of expressing current sources (or voltage sources) with general mathematical functions usually found within languages such as FORTRAN.

The electrical and dimensional data for typical n-channel and p-channel MOSFETs characterizing 4000 series CMOS devices were taken from reference [5] (these values represent circa 1983-84 design values) and input into RADSPICE. The simulation was run for I_0sec(θ)=90, 100, 110, 200 and 1000 mA, corresponding to I_0=90 mA and θ=0, 25.8, 35.1, 63.3 and 84.8 degrees (angle-of-incidence), respectively. Output waveforms (see Figure 8) produced by the simulation at NODE 2 (t=0 signifies the beginning of ion hit) show that the threshold for SEU occurs between I_0sec(θ)=90 and 100 mA (actually 96 mA). For values of peak I_0sec(θ)<96 mA, the 0 logic level at NODE 2 is preserved.

The simulated SEU threshold value of I_0=90 mA is larger than that found for current CMOS memory devices (typically I_0<1 mA [3, 4]) and is the result of several factors:

1. Reduction in cell dimensions since 1983-84, due to further increases in miniaturization and component density.

2. The dimensions used in the analysis are for 4000 series CMOS inverters and not for CMOS SRAMs. The MOSFET dimensions are likely oversized, even for SRAMs manufactured in 1983-84, because size limitations were not critical for these devices (i.e. device density was low).

3. The level of modelling used. LEVEL 2 (i.e. MOS2 Grove-Frohman or SPICE2G model) models were used for the MOSFETs, with incomplete information on some of the device parameters required for more accurate simulation. This is a relatively primitive model compared to others available in HSPICE.

If complete geometrical and electrical data were available for typical current SRAM devices, better agreement would be expected between typical experimentally measured and simulated SEU

thresholds. In the future, the SEU threshold value for typical non-rad-hard SRAMs will likely decrease further, as feature sizes are reduced and component density increases.

The SEU hardened version of the 1 bit CMOS SRAM cell appears in Figure 9. The placement of resistors in the cross-coupling lines of the inverter pair has been shown [4] to produce a SRAM with significant improvement in SEU immunity. This resistive decoupling concept is based on the principle of trying to reduce the change of the magnitude of the gate bias voltages in the "feedback loop" due to the ion-induced photocurrent. In the hardened SRAM cell during an ion strike on M4, the resistor RF1 would reduce the change in gate bias voltage at M1 and M3, thereby increasing the SEU current required to reach the threshold switching voltages of the p- and n-channel MOSFETs. Note that the values used for the feedback resistors in the simulation were RF1=RF2=150 ohms.

Output waveforms produced at NODE 2 by the RADSPICE simulation of the ion strike on the hardened SRAM cell are shown in Figure 10. These simulations were performed with $I_0\sec(\theta)$=90, 210, 220, 300 and 1000 mA, corresponding to I_0=90 mA and θ=0, 64.6, 65.9, 72.5 and 84.8 degrees (angle-of-incidence), respectively. The simulation data, shown in Figure 10, indicates that the SEU threshold for the hardened SRAM cell is between $I_0\sec(\theta)$=210 and 220 mA (actually 217 mA).

Comparison of the simulation results for the SEU threshold (based on the product $I_0\sec(\theta)$) of the non-rad-hard versus hardened circuit indicate that the hardened circuit is less sensitive to SEU photocurrent by a factor of 2.3. From another perspective, the angle-of-incidence for the same energy ion has increased from 20.4° ($I_0\sec(\theta)$=96 mA) to 65.5° ($I_0\sec(\theta)$=217 mA), thereby decreasing the probability of an SEU-producing ion interaction. The SEU threshold can be increased even further by making the values of RF1 and RF2 larger. The simulated SEU threshold for RF1=RF2=250 ohms required an $I_0\sec(\theta)$ in excess of 1500 mA (a factor of 15.6 improvement), however, normal circuit operation is degraded with increasing feedback resistance. The increased feedback resistance increases the MOSFET switching delays in the feedback loop, thereby increasing the access time (read and write) of the SRAM - an undesirable side-effect, as the quest for faster memory for modern microprocessors continues.

However, evidence exists in the literature [4] that feedback resistances as high as 50 kilohms have little effect on the access time of certain hardened SRAM designs.

4.0 CONCLUSIONS

The p-n junction photocurrent modelling techniques available in the circuit simulation code HSPICE/RADSPICE have been discussed. Example simulations have been presented for each of the p-n junction photocurrent models used in RADSPICE, with the results compared with theoretical values. The areas of applicability of the photocurrent models (including model limitations) and calculational procedures used to determine some of the critical input parameters have also been discussed.

The electrical diode device models used for the simulations in this report are LEVEL 1 models - the simplest level available. This level of device model was utilized in RADSPICE because it requires the minimum input of both physical and electrical data, most of which is normally accessible to anyone with moderately sophisticated electronics laboratory instrumentation or detailed device data sheets. In order to accurately model the response of commercially available semiconductor devices to nuclear radiation, more sophisticated models (such as the diode LEVEL 3 geometrical model) are necessary. It is impossible to employ this level of modelling without detailed knowledge of the device geometry, composition and device physics. Some of this information can be extracted through more complex semiconductor test and measurement instrumentation, or through reverse-engineering techniques. A large portion of the required semiconductor data is prohibitively difficult and time-consuming to obtain through measurement. Semiconductor manufacturers consider much of this data proprietary and are, therefore, reluctant to release it (even with the offer of signing non-disclosure agreements). The only alternative to this situation is to have custom test devices fabricated, where critical device parameters can be specified or obtained without restriction. This would satisfy both experimental and computer simulation requirements for studies of radiation effects on electronics.

A simple but effective method of radiation hardening CMOS static random-access memories (SRAMs) against single-event upset

(SEU) has been demonstrated. Techniques have been illustrated for determining SEU thresholds for the 1 bit unit SRAM memory cell for both the non-rad-hard and hardened versions. Photocurrent modelling techniques demonstrated in this example are, in general, applicable to any SPICE code.

RADSPICE can provide the radiation effects analyst with a productive simulation tool for analyzing semiconductor response to nuclear and space radiation effects and for designing rad-hard active semiconductor components at the component, circuit and system level. The user requires a knowledge of the radiation models used within the RADSPICE code, their limitations and range of applicability to effectively apply RADSPICE .

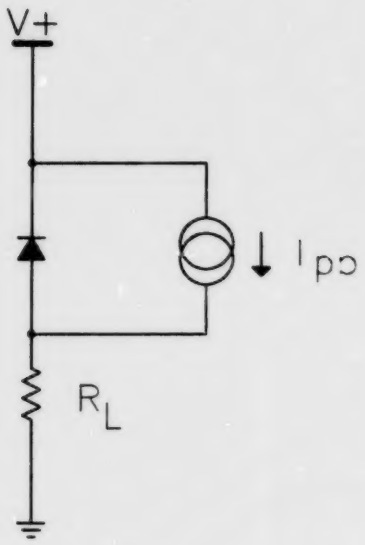

Figure 1. Schematic illustration of the approach to photocurrent modelling in p-n junctions employed by RADSPICE simulation code.

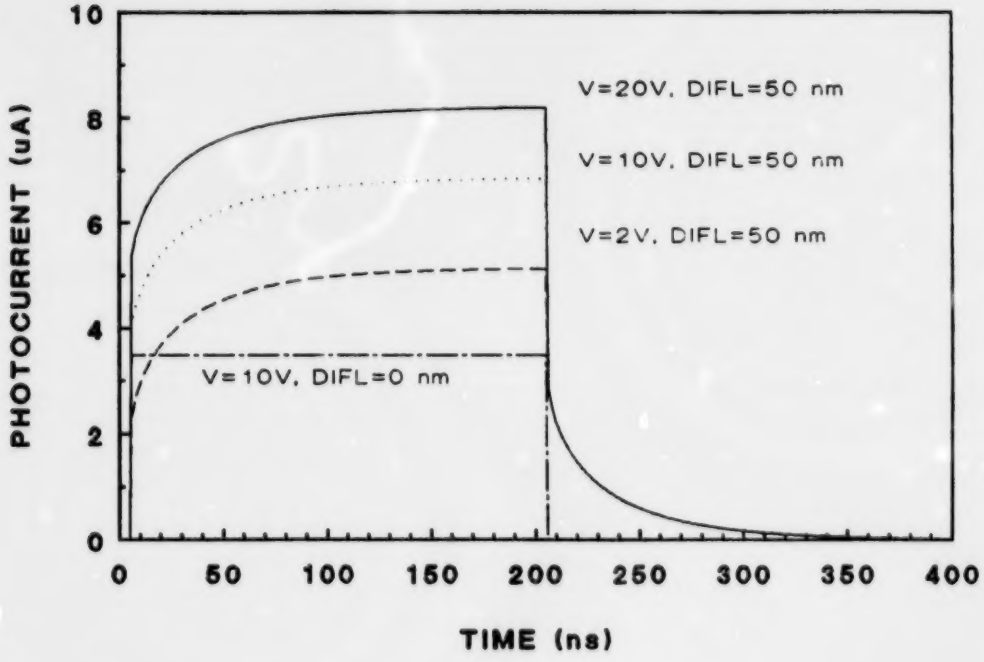

Figure 2. Results of the RADSPICE photocurrent simulation for a reverse biassed diode (zero load resistance) using the Wirth-Rogers photocurrent model [1]. See text for a description of the simulation parameters.

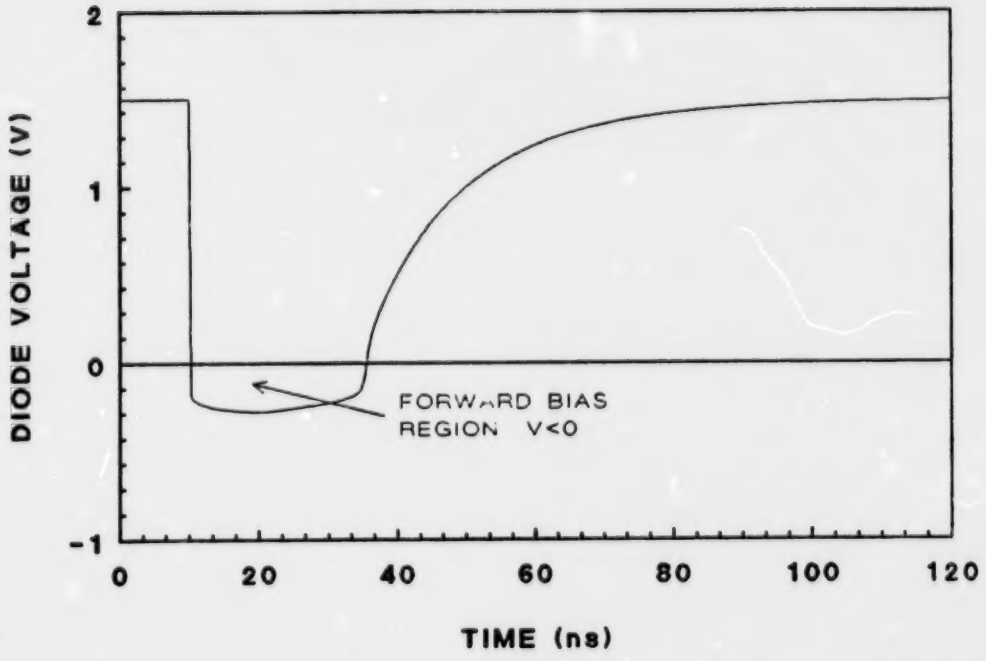

Figure 3. Photocurrent simulation results for a reverse biassed diode in series with a 200 ohm load resistance, illustrating that the Wirth-Rogers photocurrent model should not have been used due to a non-constant junction potential during the ionizing radiation pulse.

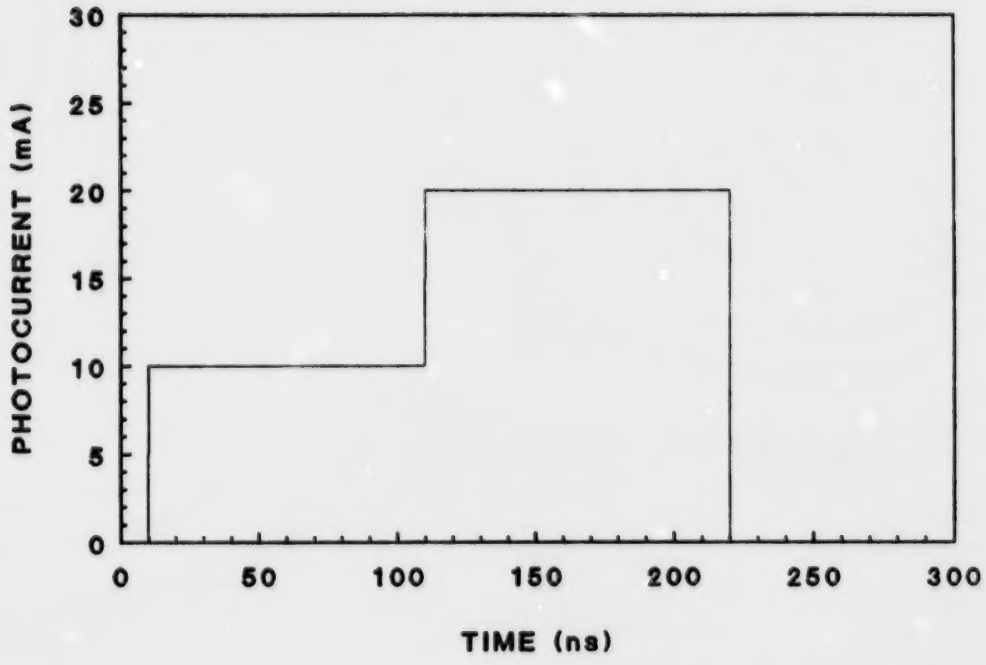

Figure 4. RADSPICE photocurrent simulation results for a reverse biassed diode (zero load resistance) using a user-defined (empirical) photocurrent model (RLEV=3). See text for a description of the simulation parameters.

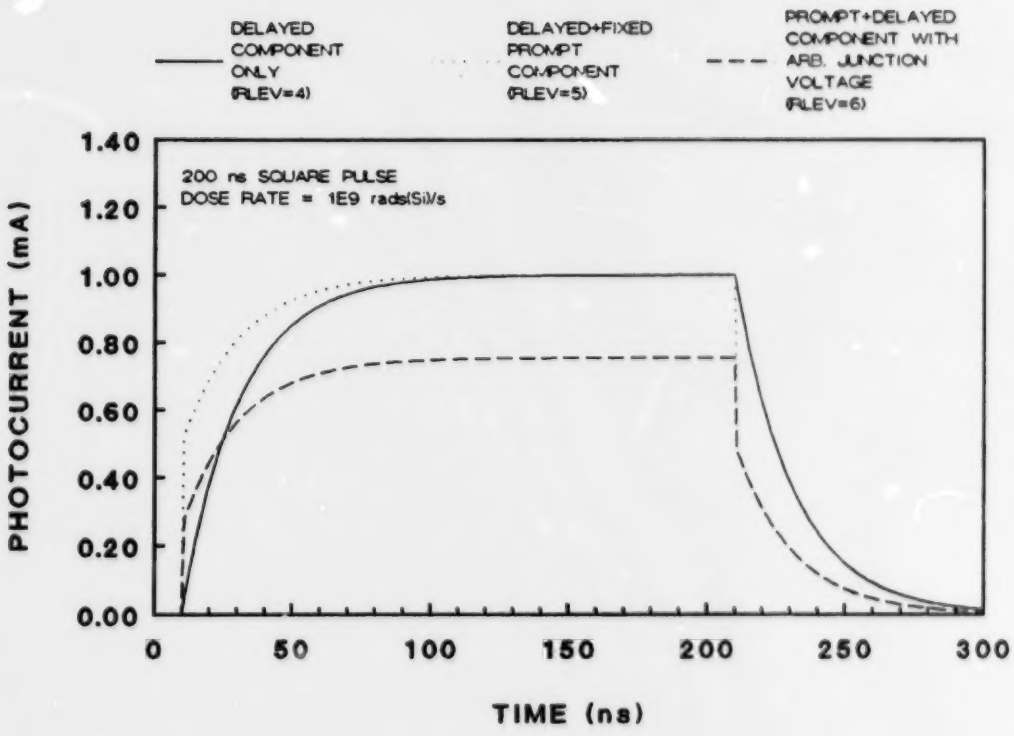

Figure 5. Photocurrent simulation results for a reverse biassed diode (zero load resistance) using three semi-empirical photocurrent models available in RADSPICE (RLEV=4, 5, and 6). See text for a description of the simulation parameters.

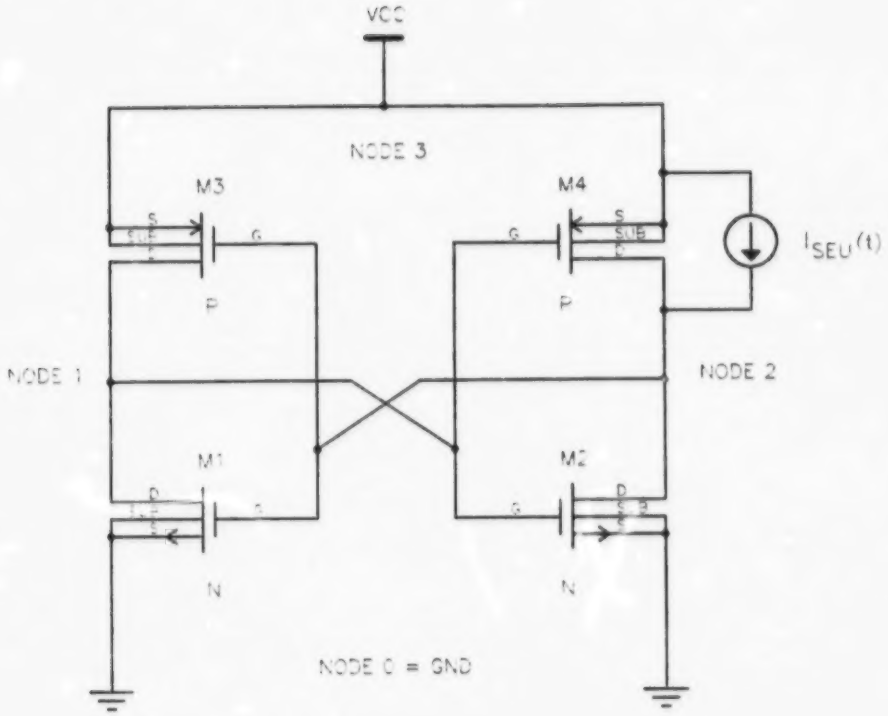

Figure 6. Schematic diagram of a typical non-rad-hard, 1 bit CMOS static random access memory (SRAM) cell. The support circuitry necessary for reading, writing and addressing the cell is not shown.

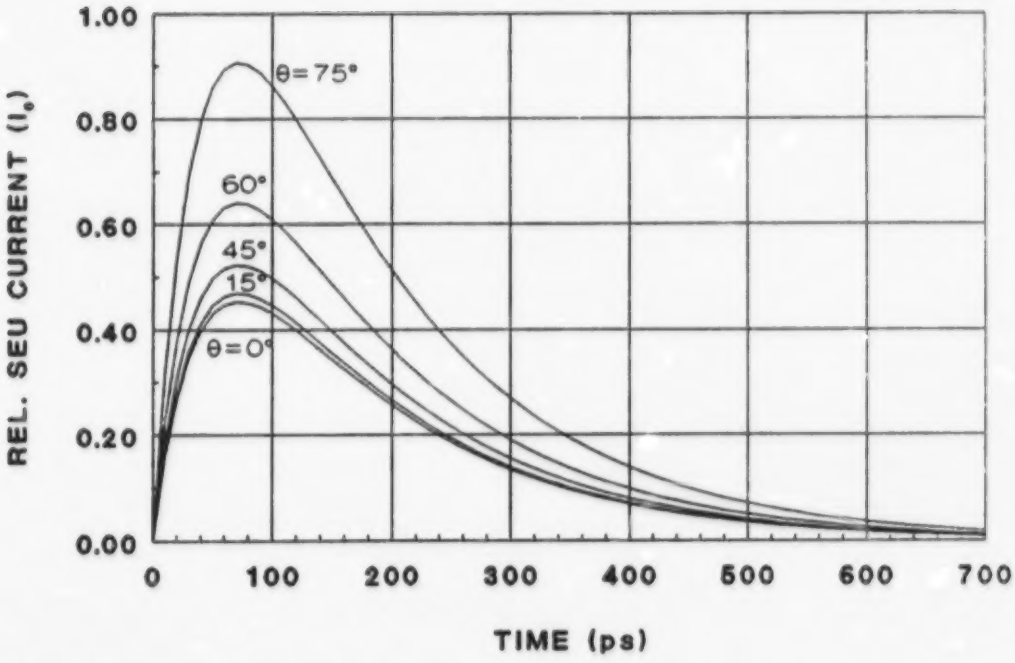

Figure 7. Photocurrent pulse generated by an ion traversing the sensitive volume of the MOSFET, as a function of angle of incidence (θ) of the ion with the surface of the SRAM. The photocurrent functions are normalized to the θ=0 curve.

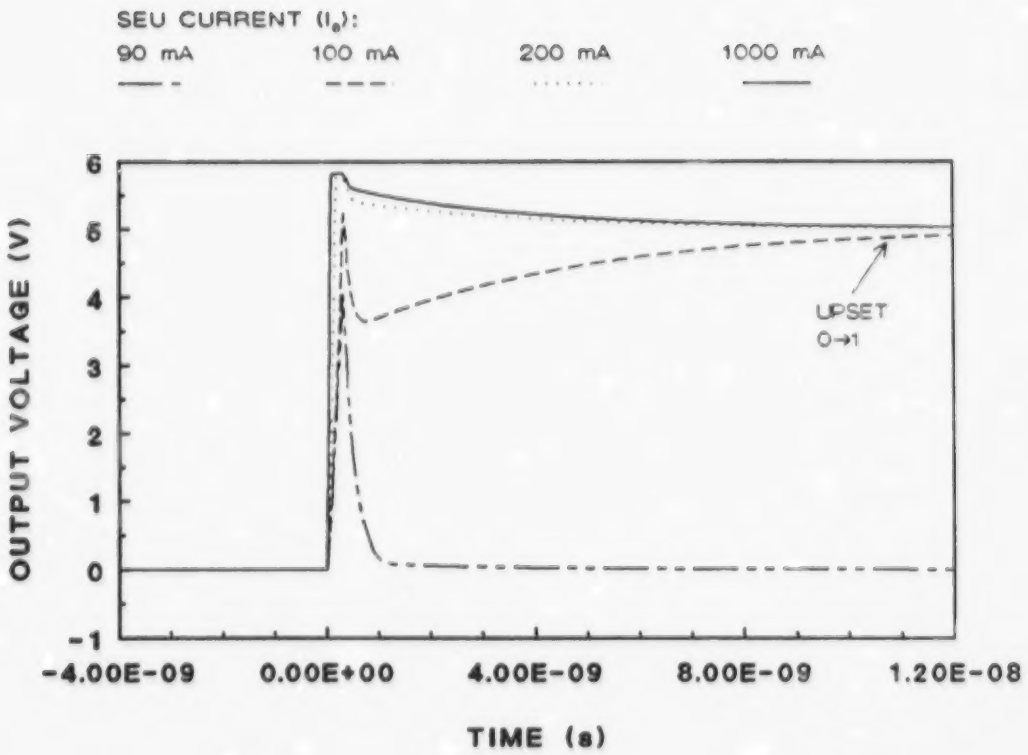

Figure 8. Simulation results of an SEU hit (commencing at t=0 s) on the non-rad-hard, 1 bit CMOS SRAM cell as a function of peak SEU current. The output waveform reflects the logic level, or data stored within the cell, at NODE 2. The SEU threshold current was determined to be approximately 96 mA.

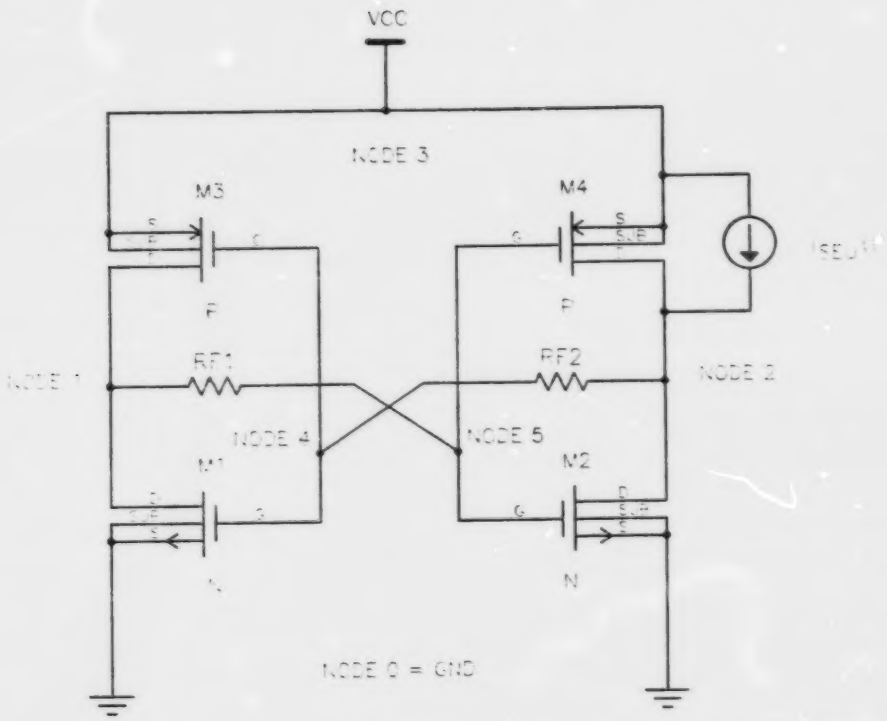

Figure 9. Schematic diagram of a 1 bit CMOS SRAM cell that has been hardened against single-event upset by the addition of feedback or decoupling resistors.

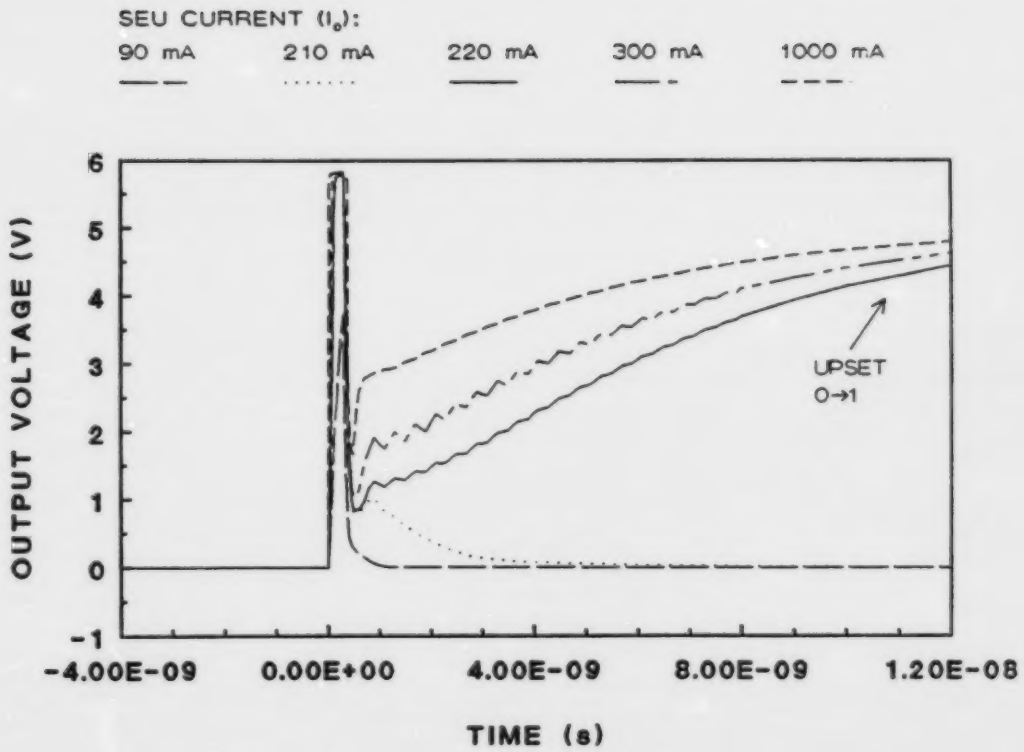

Figure 10. Simulation results of an SEU hit (commencing at t=0 s) on the hardened, 1 bit CMOS SRAM cell as a function of peak SEU current. The output waveform reflects the logic level, or data stored within the cell, at NODE 2. The SEU threshold current was determined to be approximately 217 mA, which is a factor of 2.3 larger than the non-rad-hard version.

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(U) Computer simulation of radiation effects in electronics is an important research and engineering tool for understanding the interaction of nuclear and space radiation in semiconductor devices and for developing rad-hard electronics at the device, circuit and system level. This report investigates the photocurrent modelling capability of a commercially available SPICE circuit simulation code (RADSPICE) that has integrated radiation effects modelling capability. Specifically, the various models for photocurrent generation in p-n junctions from pulses of ionizing radiation are discussed and sample simulations are provided for each of the photocurrent models. The simulation results are compared with theoretical values and the limitations of the models and range of applicability are discussed.

(U) Single-event upset (SEU) modelling in a CMOS static random access memory (SRAM) is illustrated using photocurrent simulation techniques. A corresponding rad-hard version of the SRAM is demonstrated. RADSPICE simulation results for both non-rad-hard and rad-hard SRAM designs are evaluated, thereby providing a means of estimating SEU vulnerability.

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